CLAIMS

What is claimed is:

1. A hybrid substrate comprising:

a first semiconductor layer having a first crystallographic orientation; and

a second semiconductor layer having a second crystallographic orientation which is different from the first crystallographic orientation, wherein said first and second semiconductor layers are separated from each other by a conductive interface.

2. The hybrid substrate of Claim 1 wherein said conductive interface comprises a hydrophilic surface of at least one of said semiconductor layers.

3. The hybrid substrate of Claim 1 wherein said conductive interface comprises a hydrophobic surface of at least one of said semiconductor layers.

4. The hybrid substrate of Claim 1 wherein said first semiconductor layer and the second semiconductor layer are composed of the same or different semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, other III/V or II/VI compound semiconductors and any combination thereof.

5. The hybrid substrate of Claim 1 wherein said first semiconductor layer and the second semiconductor layer are both composed of Si.

6. The hybrid substrate of Claim 1 wherein said first semiconductor layer has a (100) crystal orientation and said second semiconductor layer has a (110) crystal orientation.

7. The hybrid substrate of Claim 1 wherein said first semiconductor layer has a (110) crystal orientation and said second semiconductor layer has a (100) crystal orientation.

8. The hybrid substrate of Claim 1 wherein said first semiconductor layer comprises a relaxed semiconductor material or a stack of a relaxed semiconductor material and a strained semiconductor material.

9. The hybrid substrate of Claim 1 wherein said second semiconductor material comprises a relaxed semiconductor material or a stack of a relaxed semiconductor material and a strained semiconductor material.

10. A method of fabricating a hybrid substrate comprising:

providing a first semiconductor wafer comprising a first semiconductor material having a first crystallographic orientation and a second semiconductor wafer comprising a second semiconductor material having a second crystallographic orientation which is different from the first crystallographic orientation; and

bonding the first semiconductor wafer to the second semiconductor wafer, wherein a conductive interface forms between the wafers.

11. The method of Claim 10 further comprising treating a surface of at least one of the wafers to provide a hydrophobic or hydrophilic surface for bonding.

12. The method of Claim 11 wherein said treating comprises a HF dip process.

13. The method of Claim 11 wherein said treating comprises a dry clean process, an argon high-energy surface etch, a wet chemical oxidizing acid or any combination thereof.

14. The method of Claim 10 wherein said bonding comprising contacting the two wafers at nominal room temperature.

15. The method of Claim 14 further comprising applying an external force during said contacting.

16. The method of Claim 10 further comprising an annealing step following said bonding.

17. The method of Claim 16 wherein said annealing is performed at a temperature from about 900° to about 1300°C.

18. The method of Claim 16 wherein said annealing is performed in $O_2$, $N_2$, Ar or a low vacuum.

19. The method of Claim 16 wherein said annealing is performed at a temperature of less than 900°C.

20. The method of Claim 10 wherein said second semiconductor wafer is obtained by a layer transfer technique.

21. The method of Claim 10 wherein said second semiconductor wafer comprises an implant region and following said bonding a heating step and a layer spitting anneal are performed.

22. The method of Claim 10 wherein said first semiconductor wafer has a (100) crystal orientation and said second semiconductor wafer has a (110) crystal orientation.

23. The method of Claim 10 wherein said first semiconductor wafer has a (110) crystal orientation and said second semiconductor wafer has a (100) crystal orientation.

24. An integrated semiconductor structure comprising:

a hybrid structure comprising a first device region having a first crystallographic orientation and a second device region having a second crystallographic orientation, said first crystallographic orientation is different from said second crystallographic orientation;

an isolation region separating said first device region from said second device region; and

at least one first semiconductor device located in said first device region and at least one second semiconductor device located in said second device region, wherein said first semiconductor device and said second semiconductor device are both bulk-like devices and both devices contain a well region that serves as a body contact.

25. The integrated semiconductor structure of Claim 24 wherein the first crystallographic orientation is (110) and the second crystallographic orientation is (100).

26. The integrated semiconductor structure of Claim 25 wherein said at least one first semiconductor device is a pFET and the at least one second semiconductor device is an nFET.

27. The integrated semiconductor structure of Claim 24 wherein the first crystallographic orientation is (100) and the second crystallographic orientation is (110).

28. The integrated semiconductor structure of Claim 27 wherein said at least one first semiconductor device is an nFET and the at least one second semiconductor device is a pFET.

29. The integrated semiconductor structure of Claim 24 wherein the first device region includes a regrown semiconductor material located atop a first semiconductor material,

said regrown semiconductor material having the same crystallographic orientation as the first semiconductor material.

30. The integrated semiconductor structure of Claim 29 wherein said regrown semiconductor material is recessed and another semiconductor material is formed atop the recessed regrown semiconductor material.

31. The integrated semiconductor structure of Claim 30 wherein said another semiconductor material is a strained semiconductor or a stack comprising a relaxed semiconductor and a strained semiconductor.

32. The integrated semiconductor structure of Claim 29 wherein said regrown semiconductor material is a semiconductor selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, other III/V or II/VI compound semiconductors and any combination thereof.

33. The integrated semiconductor structure of Claim 24 wherein said first and second semiconductor device regions both include strained Si.

34. The integrated semiconductor structure of Claim 29 wherein said regrown semiconductor material comprises a strained semiconductor layer located atop a relaxed semiconductor layer.

35. The integrated semiconductor structure of Claim 24 wherein said hybrid structure comprising a hybrid substrate that comprises a first semiconductor layer having a first crystallographic orientation; and a second semiconductor layer having a second crystallographic orientation which is different from the first crystallographic orientation, wherein said first and second semiconductor layers are separated from each other by a conductive interface.

36. A method of forming an integrated semiconductor structure comprising:

providing a hybrid substrate comprising at least a first semiconductor layer of a first crystallographic orientation and a second semiconductor layer of a second crystallographic orientation separated by a conducting interface, said first crystallographic orientation is different from said second crystallographic orientation and said first semiconductor layer lies below said second semiconductor layer;

selectively etching a portion of the hybrid substrate to expose a surface of the first semiconductor layer;

regrowing a semiconductor material on said exposed surface of the first semiconductor layer, said semiconductor material having a crystallographic orientation that is the same as the first crystallographic orientation;

providing well regions in said second semiconductor layer and said regrown semiconductor material; and

forming at least one first semiconductor device on said regrown semiconductor material, while forming at least one second semiconductor device on said second semiconductor layer.

37. The method of Claim 36 wherein said providing a hybrid substrate comprises providing a first semiconductor wafer comprising a first semiconductor material having a first crystallographic orientation and a second semiconductor wafer comprising a second semiconductor material having a second crystallographic orientation which is different from the first crystallographic orientation; and bonding the first semiconductor wafer to the second semiconductor wafer, wherein a conductive interface forms between the wafers.

38. The method of Claim 37 further comprising treating a surface of at least one of the wafers to provide a hydrophobic or hydrophilic surface for bonding.

39. The method of Claim 38 wherein said treating comprises a HF dip process.

40. The method of Claim 38 wherein said treating comprises a dry clean process, an argon high-energy surface etch, a wet chemical oxidizing acid or any combination thereof.

41. The method of Claim 37 wherein said bonding comprising contacting the two wafers at nominal room temperature.

42. The method of Claim 41 further comprising applying an external force during said contacting.

43. The method of Claim 37 further comprising an annealing step following said bonding.

44. The method of Claim 43 wherein said annealing is performed at a temperature from about 900° to about 1300°C.

45. The method of Claim 43 wherein said annealing is performed in $O_2$, $N_2$, Ar or a low vacuum.

46. The method of Claim 43 wherein said annealing is performed at a temperature of less than 900°C.

47. The method of Claim 37 wherein said second semiconductor wafer is obtained by a layer transfer technique.

48. The method of Claim 37 wherein said second semiconductor wafer comprises an implant region and following said bonding a heating step and a layer spitting anneal are performed.

49. The method of Claim 36 wherein said selectively etching comprising lithography and etching.

50. The method of Claim 36 wherein said regrowing comprising epitaxial growing.

51. The method of Claim 36 wherein said regrown semiconductor material is recessed and another semiconductor material is formed atop the recessed surface, said regrown semiconductor material and said another material both having the first crystallographic orientation.

52. The method of Claim 36 wherein said providing well regions comprises patterning, ion implantation and annealing.

53. The method of Claim 36 wherein the first crystallographic orientation is (110) and the second crystallographic orientation is (100).

54. The method of Claim 53 wherein said at least one first semiconductor device is a pFET and the at least one second semiconductor device is an nFET.

55. The method of Claim 36 wherein the first crystallographic orientation is (100) and the second crystallographic orientation is (110).

56. The method of Claim 55 wherein said at least one first semiconductor device is an nFET and the at least one second semiconductor device is a pFET.

57. The method of Claim 36 wherein at least one of said first semiconductor device or said second semiconductor device is formed on a strained semiconductor material.

58. The method of Claim 57 wherein said strained semiconductor material is formed atop a relaxed semiconductor material.